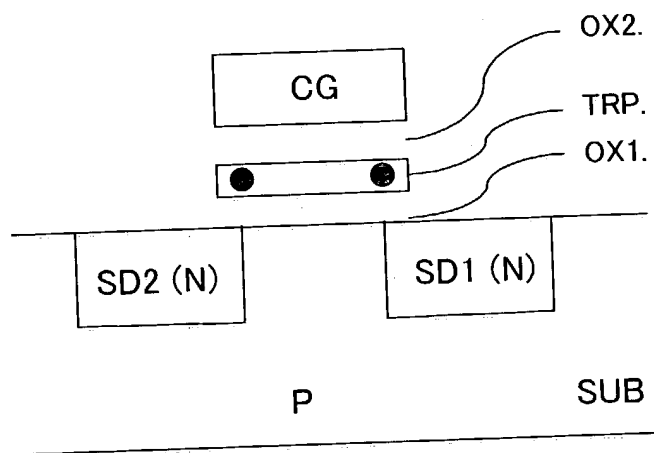
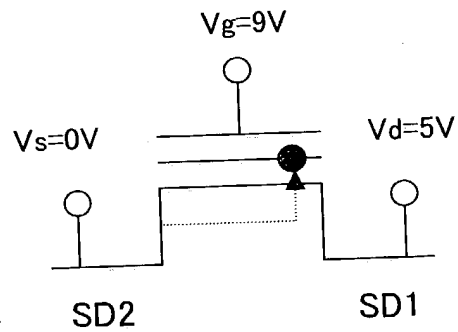


FIG. 1

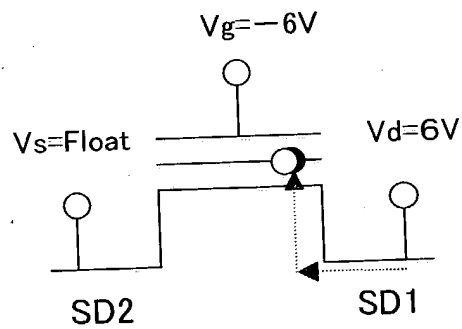


**FIG. 2**

**A. WRITE OPERATION**



**B. ERASE OPERATION**



**C. READ-OUT OPERATION**

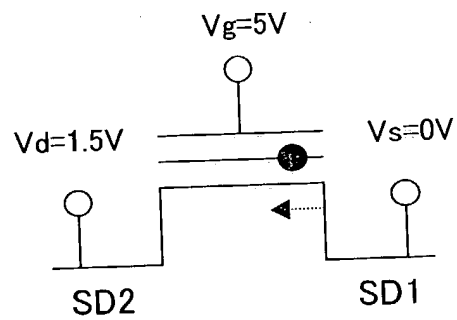


FIG. 3

PRIOR ART

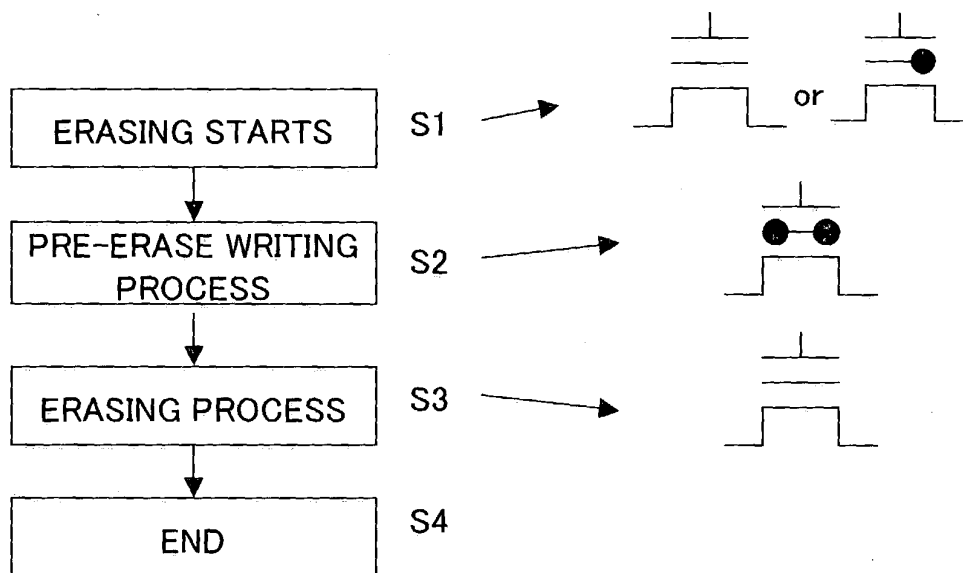
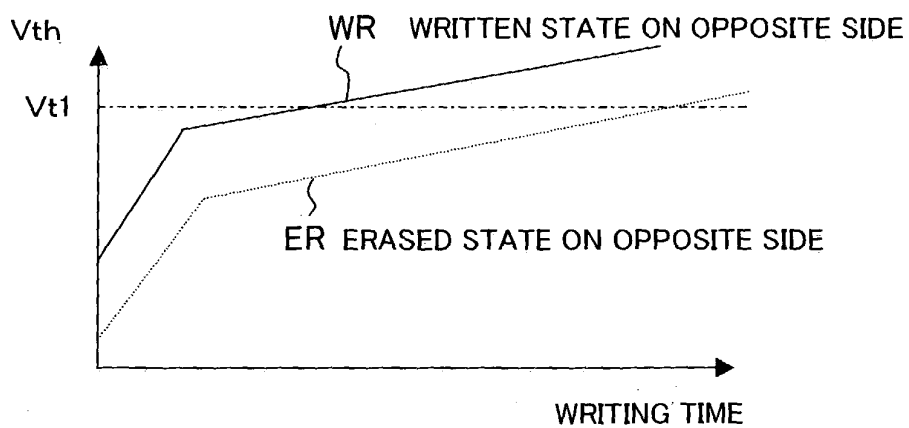
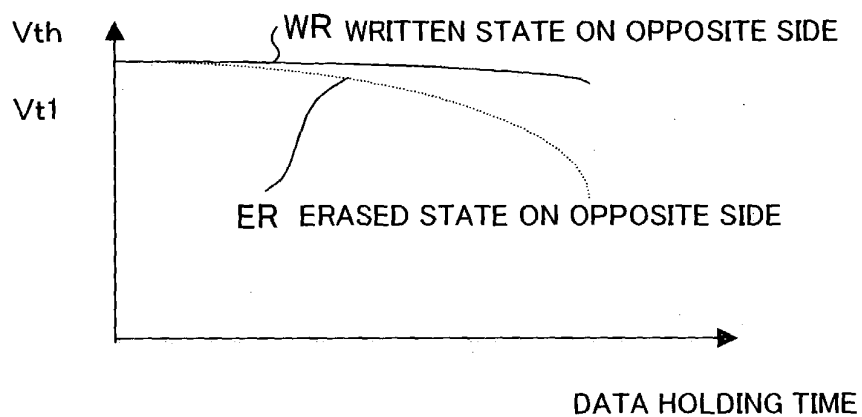


FIG. 4



**FIG. 5**



**FIG. 6**

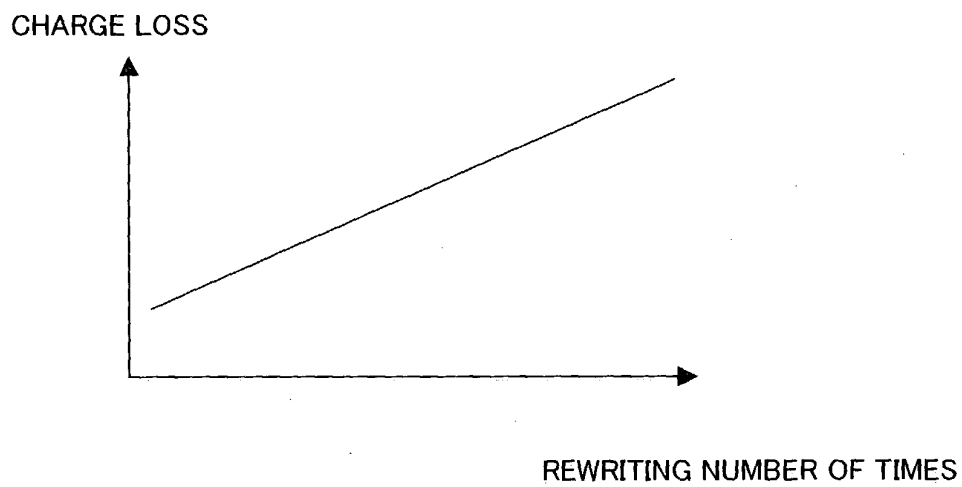


FIG. 7

NONVOLATILE MEMORY OF EMBODIMENT

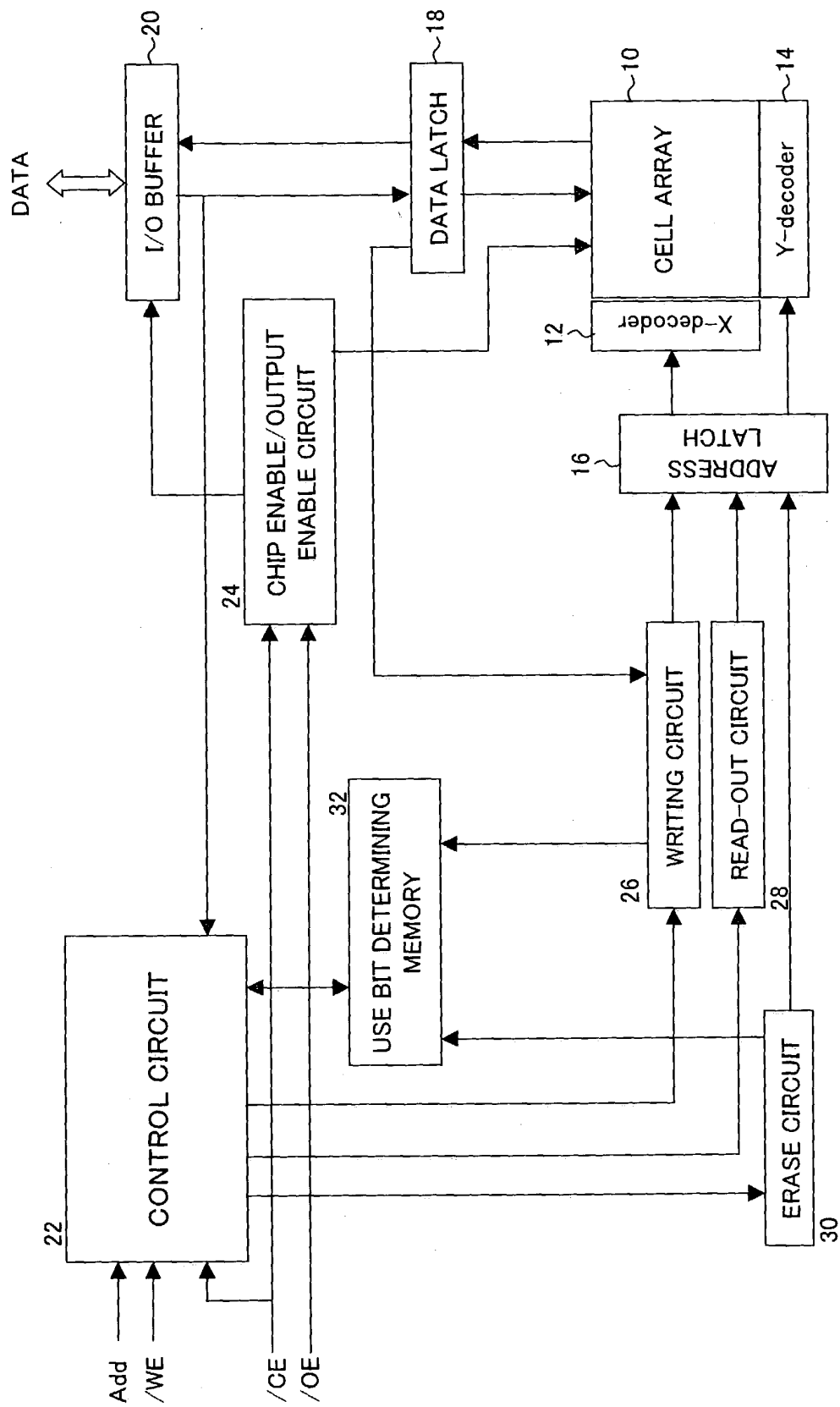


FIG. 8

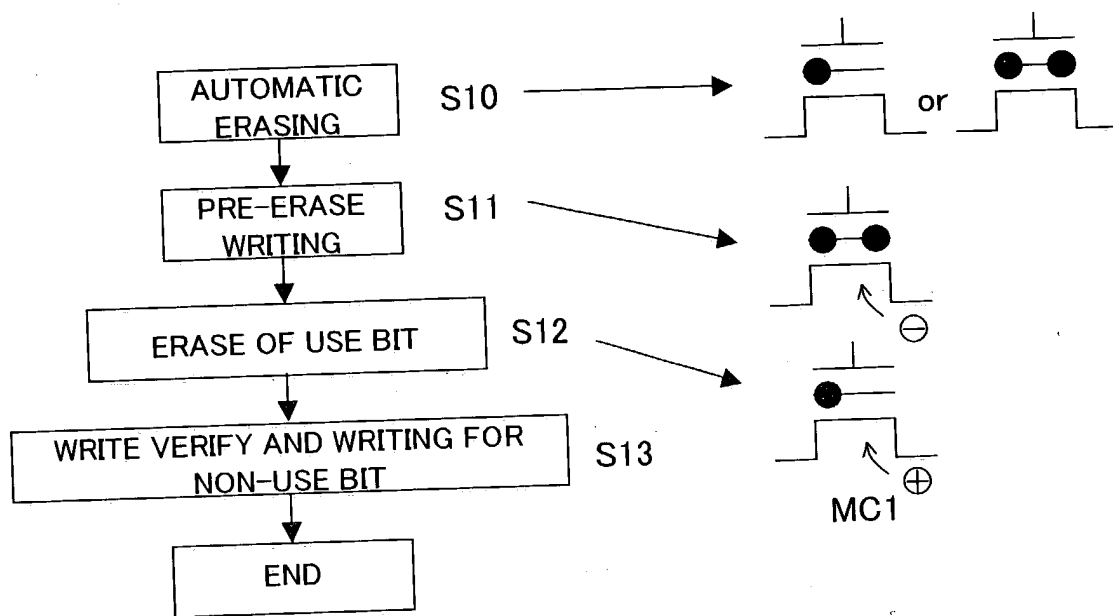


FIG. 9

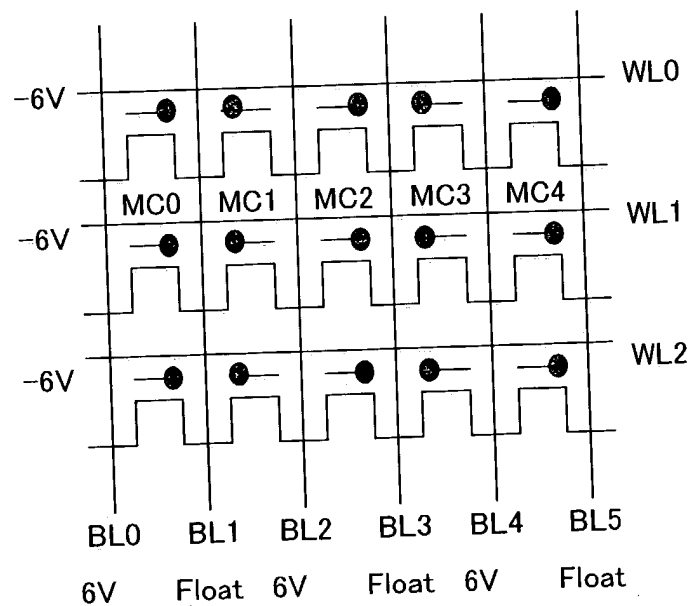


FIG. 10

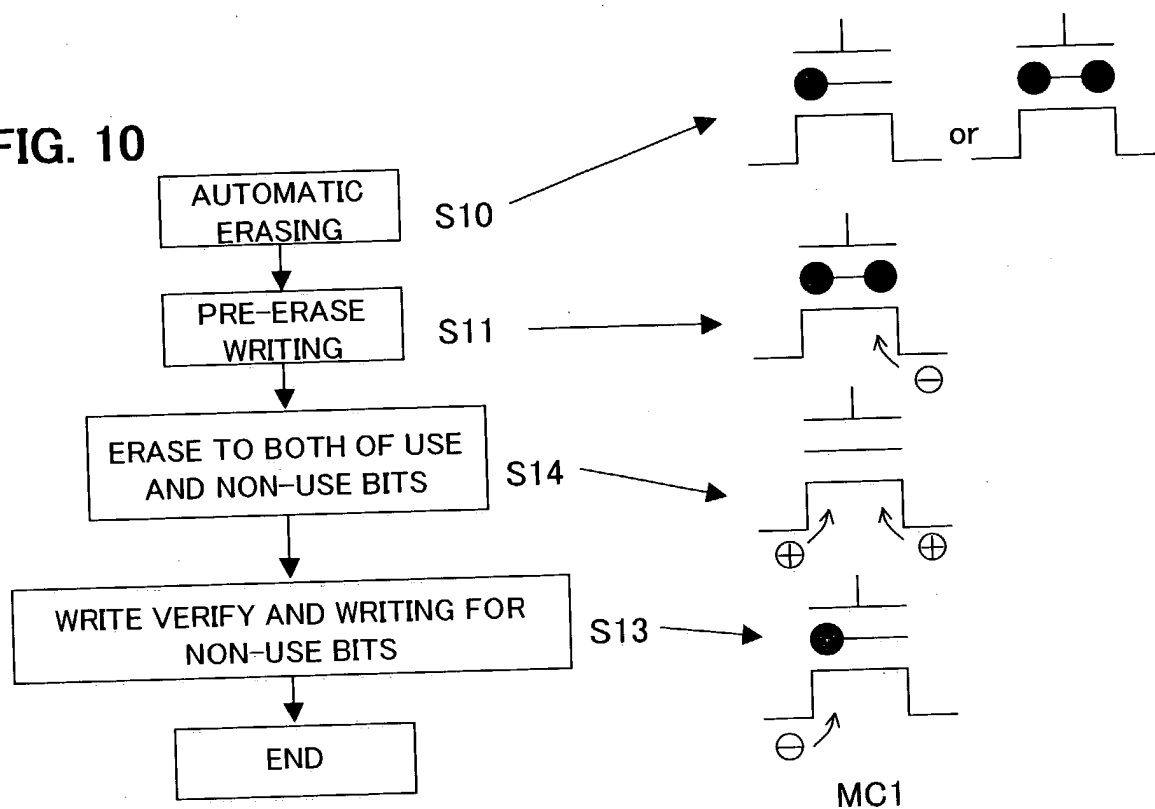


FIG. 11

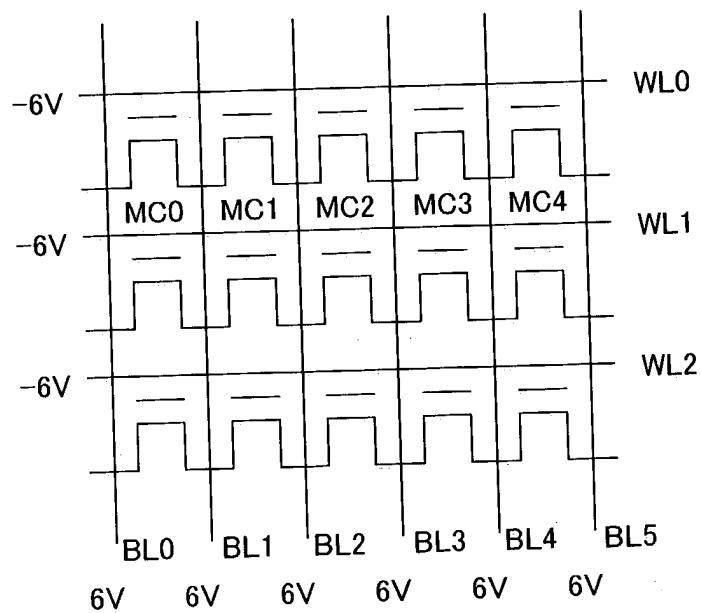


FIG. 12

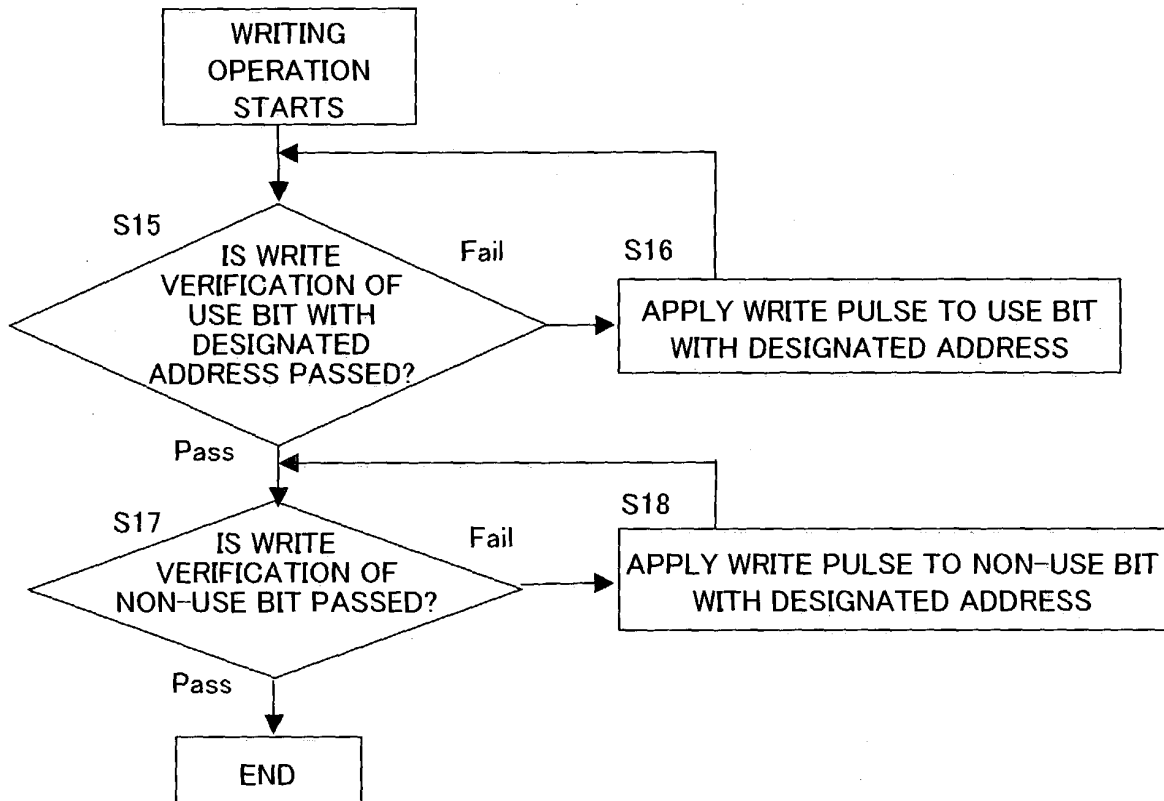


FIG. 13

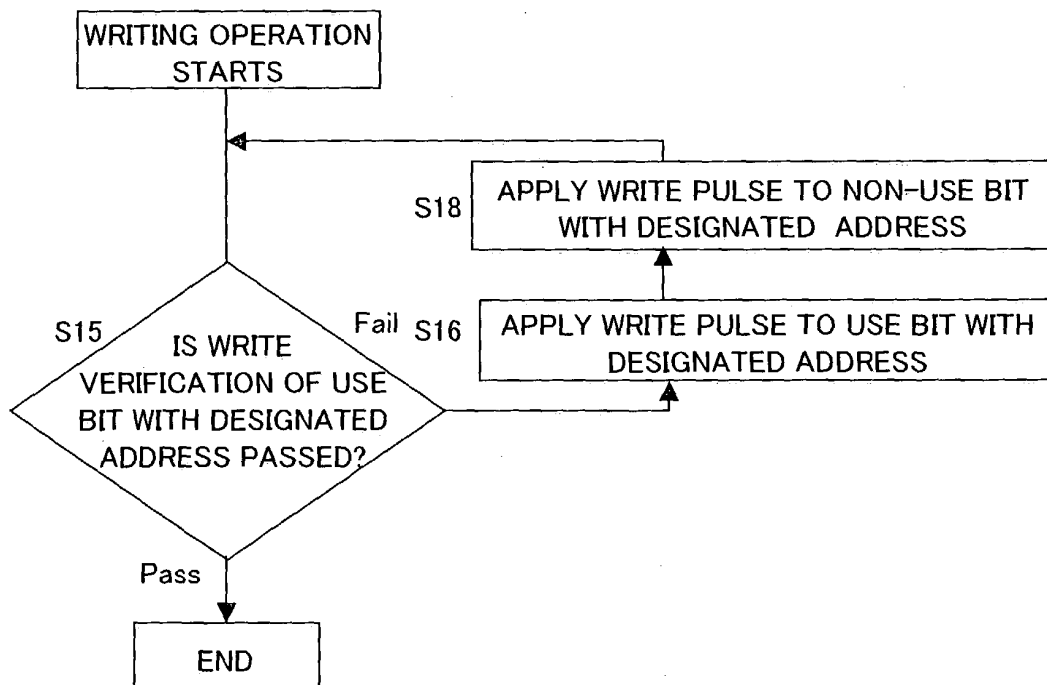
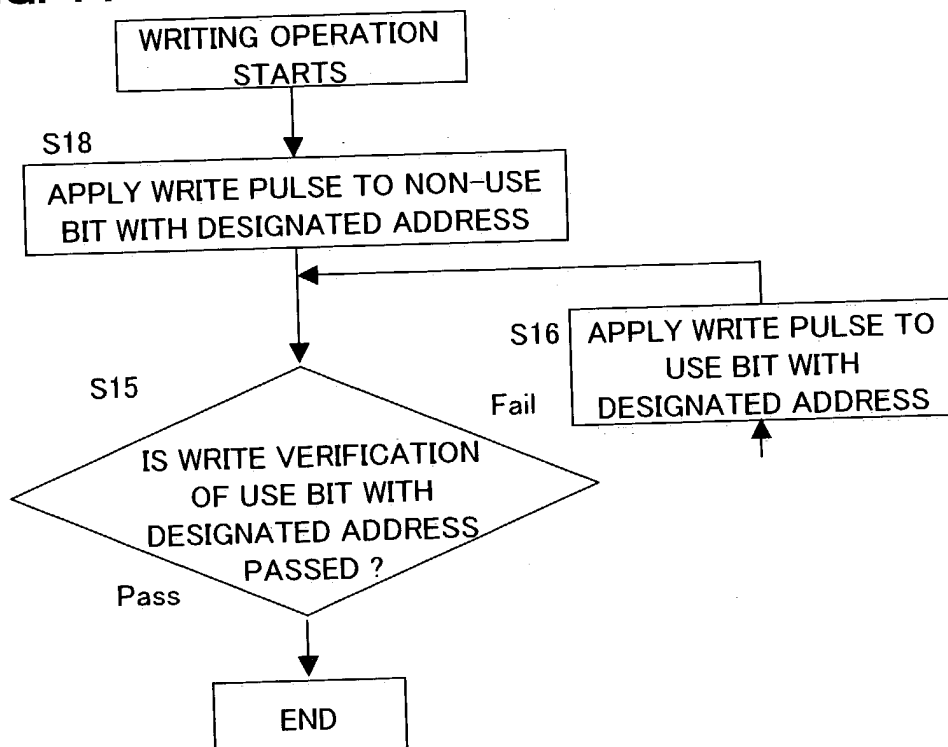


FIG. 14



# FIG. 15

AUTOMATIC ERASING OPERATION (1)  
WITH REPLACEMENT OF NON-USE BIT TO  
USE BIT, IN WHICH NON-USE BIT IS KEPT IN  
WRITTEN CONDITION

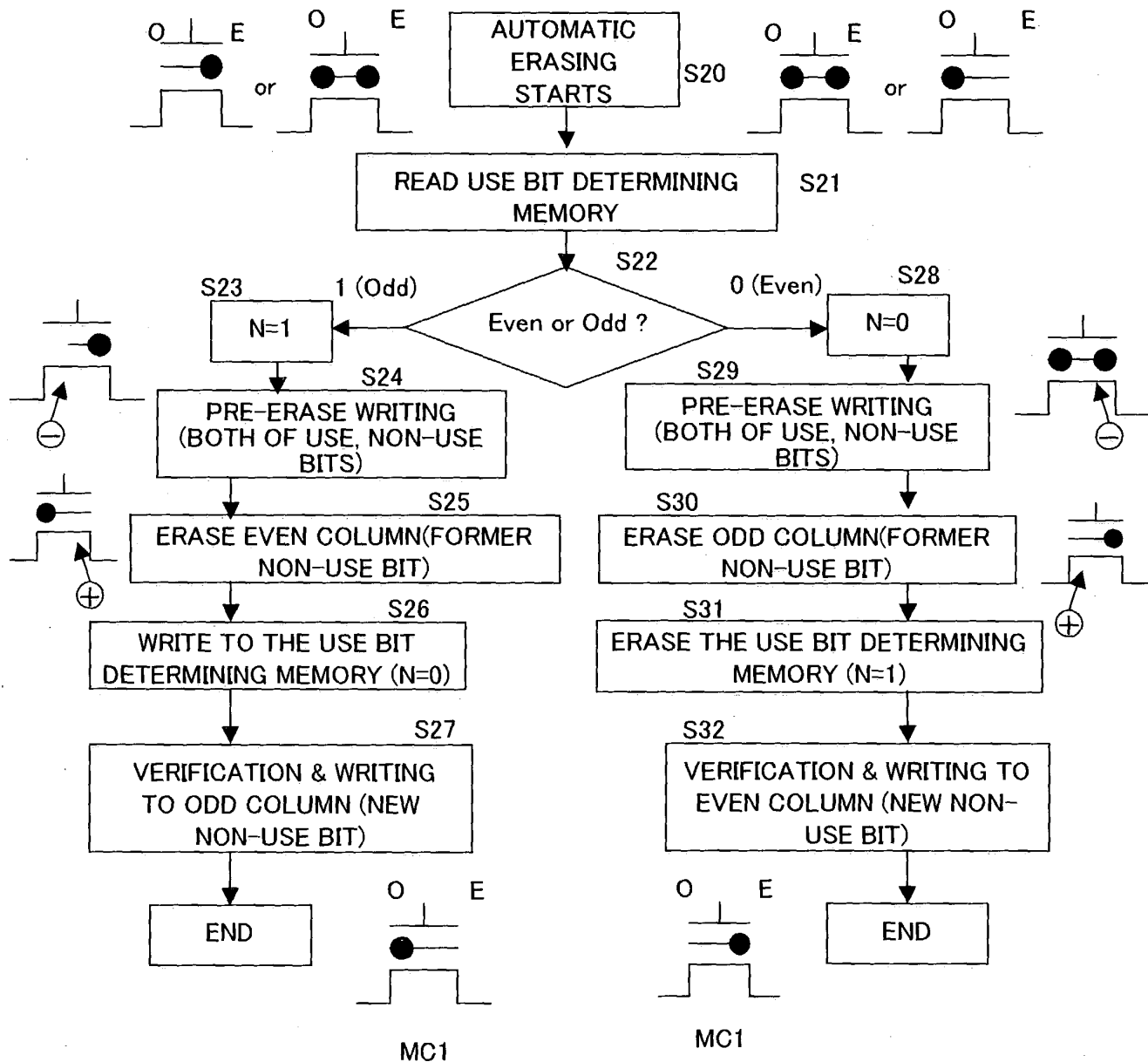
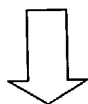
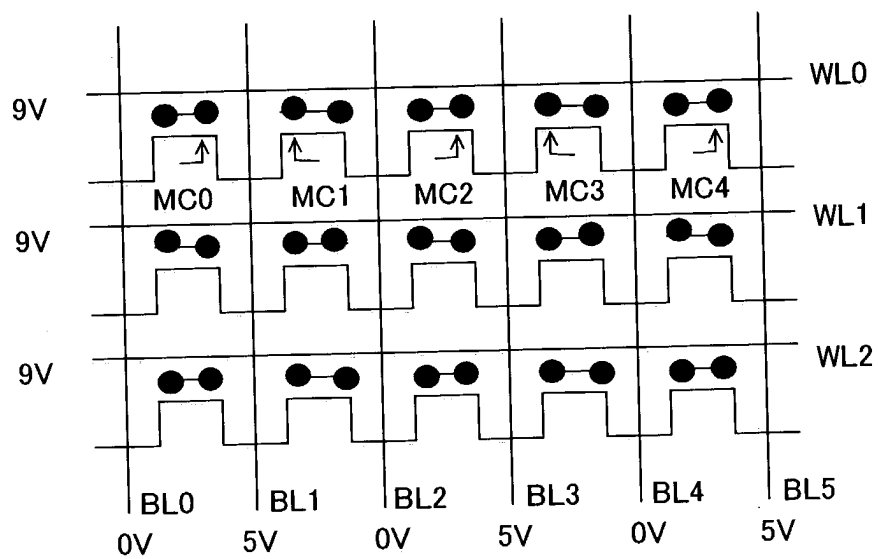


FIG. 16

S24 PRE-ERASE WRITING PROCESS



S25 ERASE PROCESS

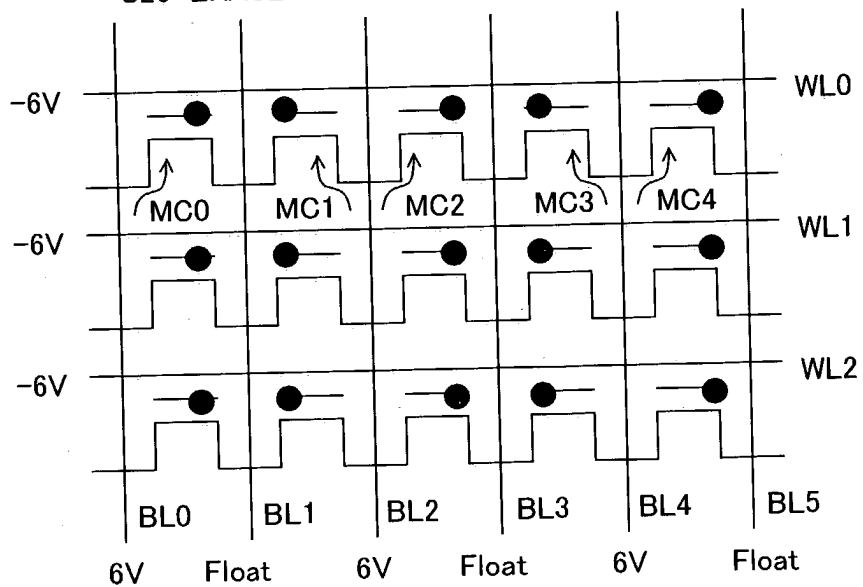
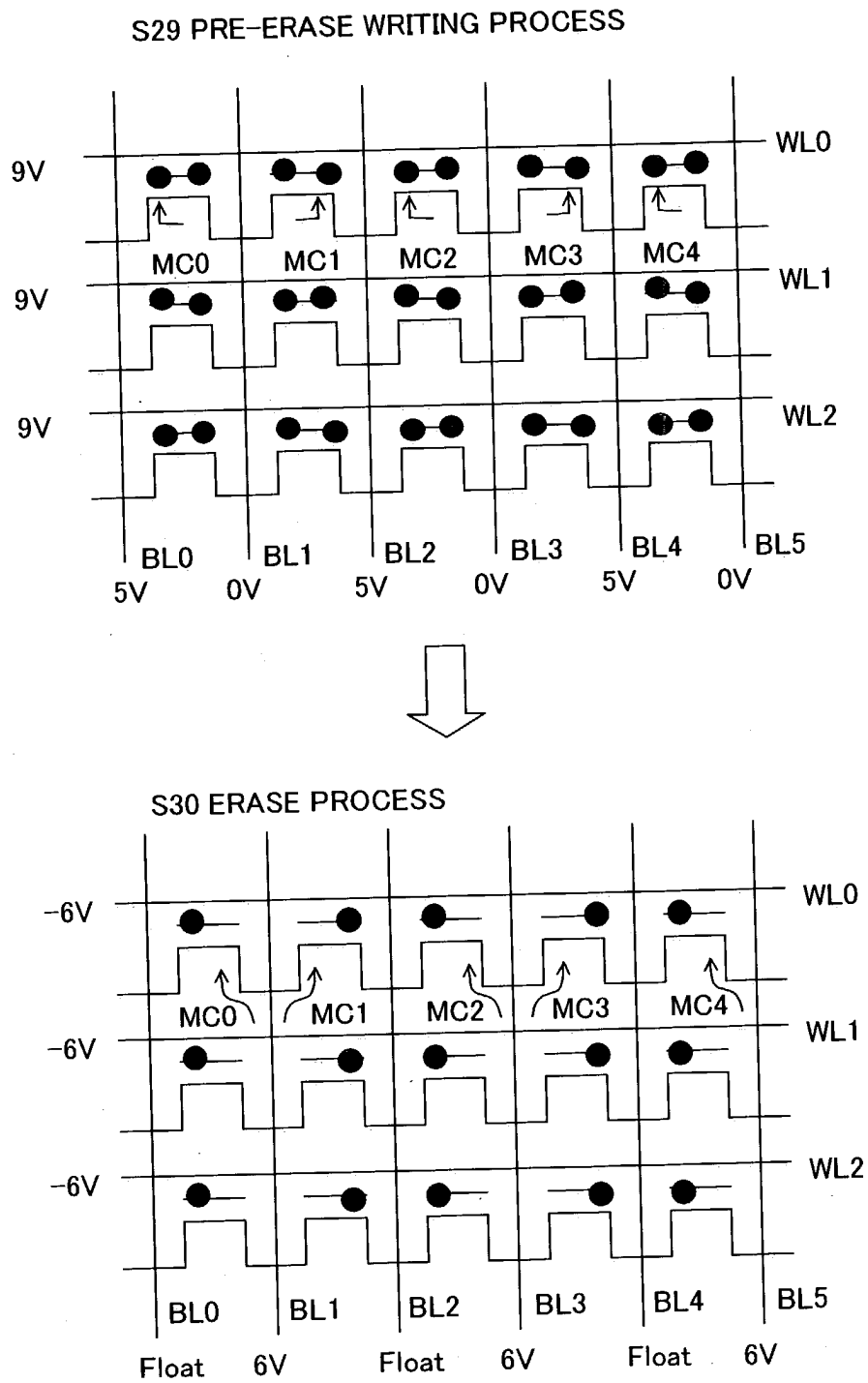
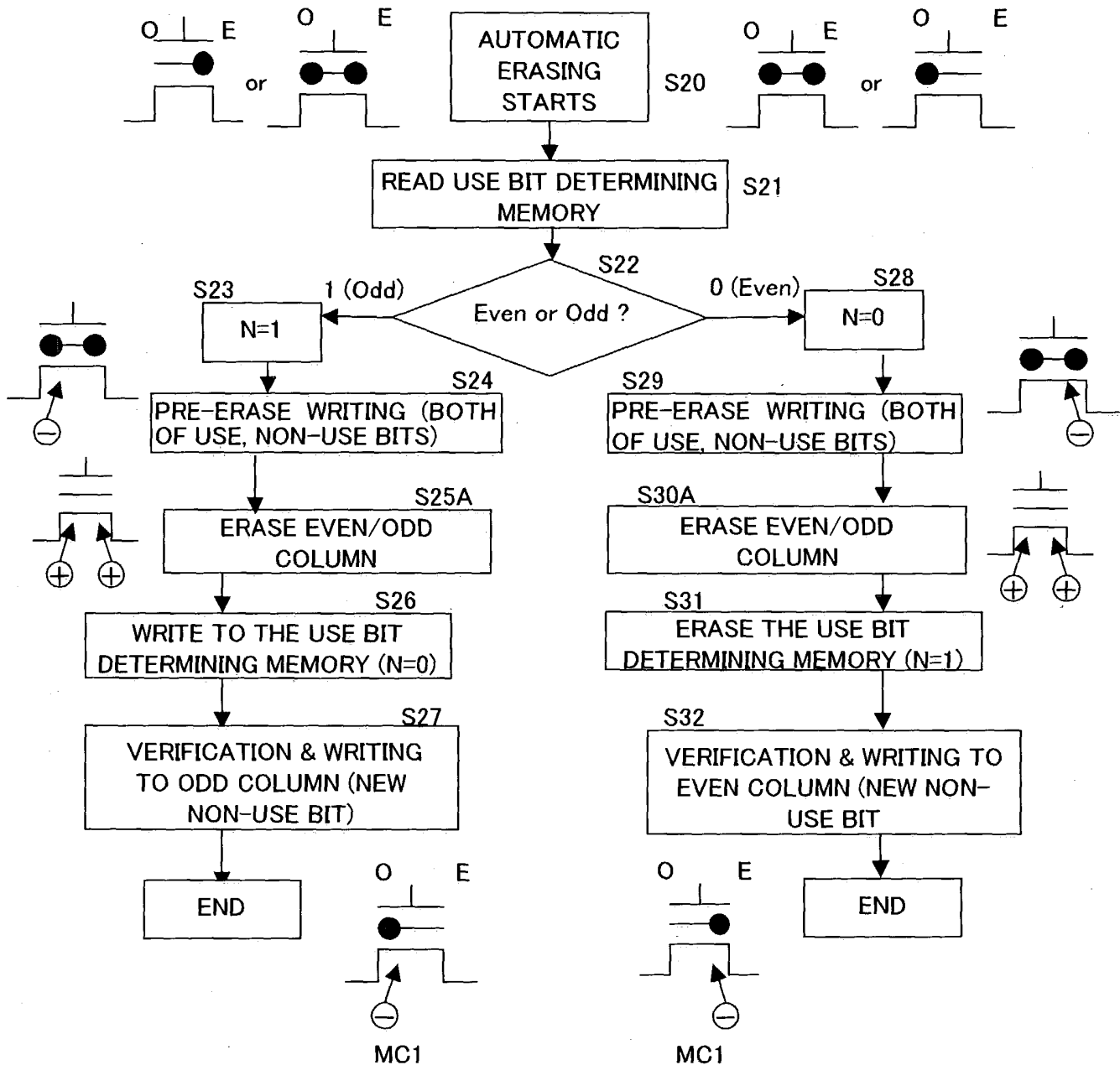


FIG. 17



**FIG. 18**

AUTOMATIC ERASING OPERATION (2)  
WITH REPLACEMENT OF NON-USE BIT  
TO USE BIT, IN WHICH NON-USE BIT IS  
KEPT IN WRITTEN CONDITION



**FIG. 19**

AUTOMATIC ERASING OPERATION (3)  
WITH REPLACEMENT OF NON-USE BIT  
TO USE BIT, IN WHICH NON-USE BIT IS  
KEPT IN WRITTEN CONDITION

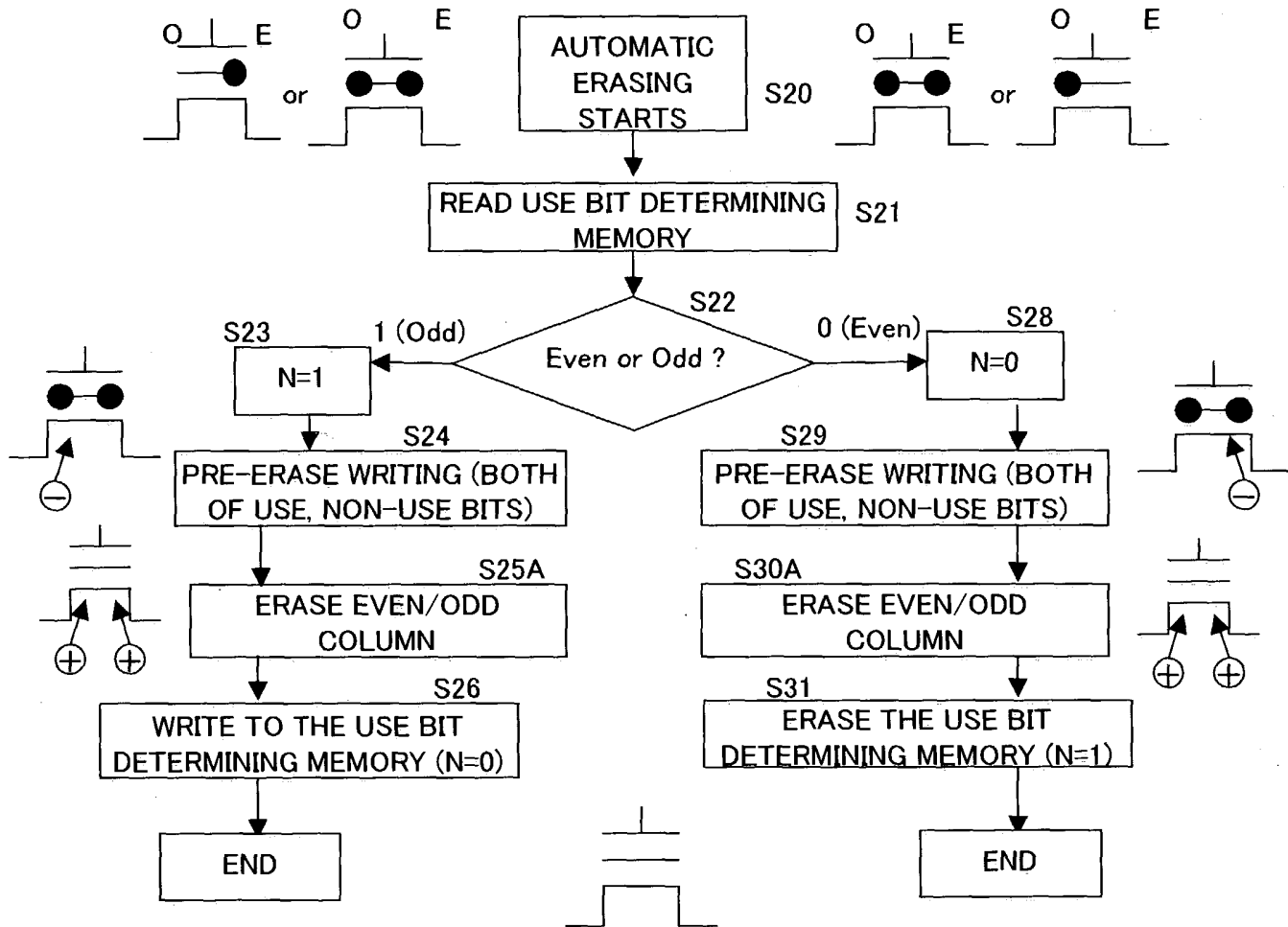
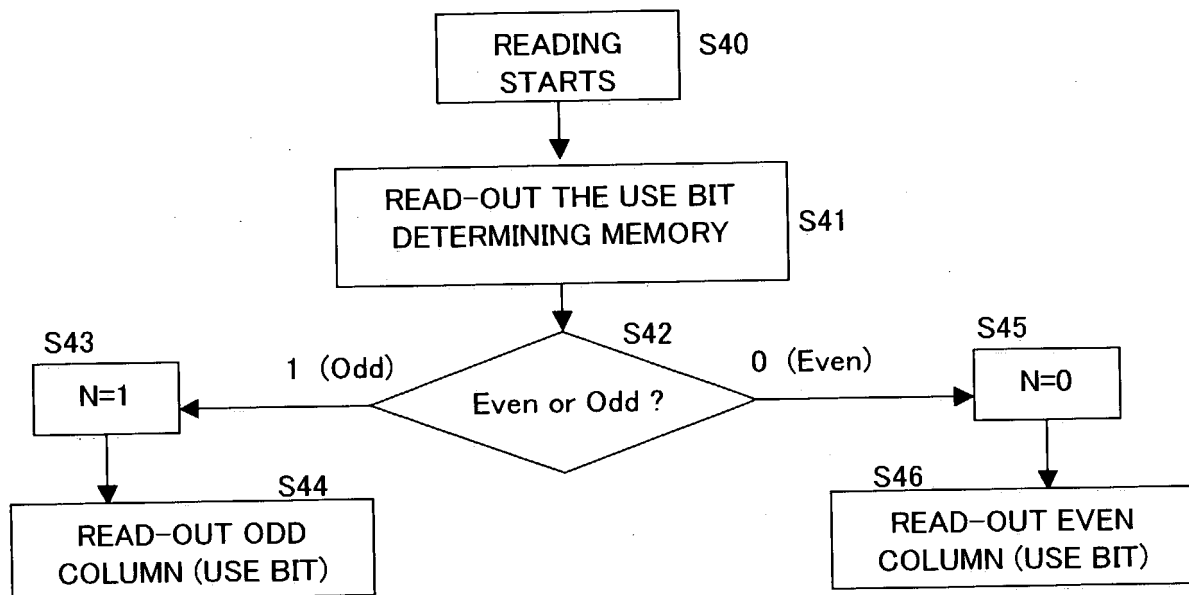


FIG. 20



**FIG. 21**

AUTOMATIC ERASING OPERATION (1)  
WITH REPLACEMENT OF NON-USE BIT  
TO USE BIT, IN WHICH NON-USE BIT IS  
KEPT IN ERASED CONDITION

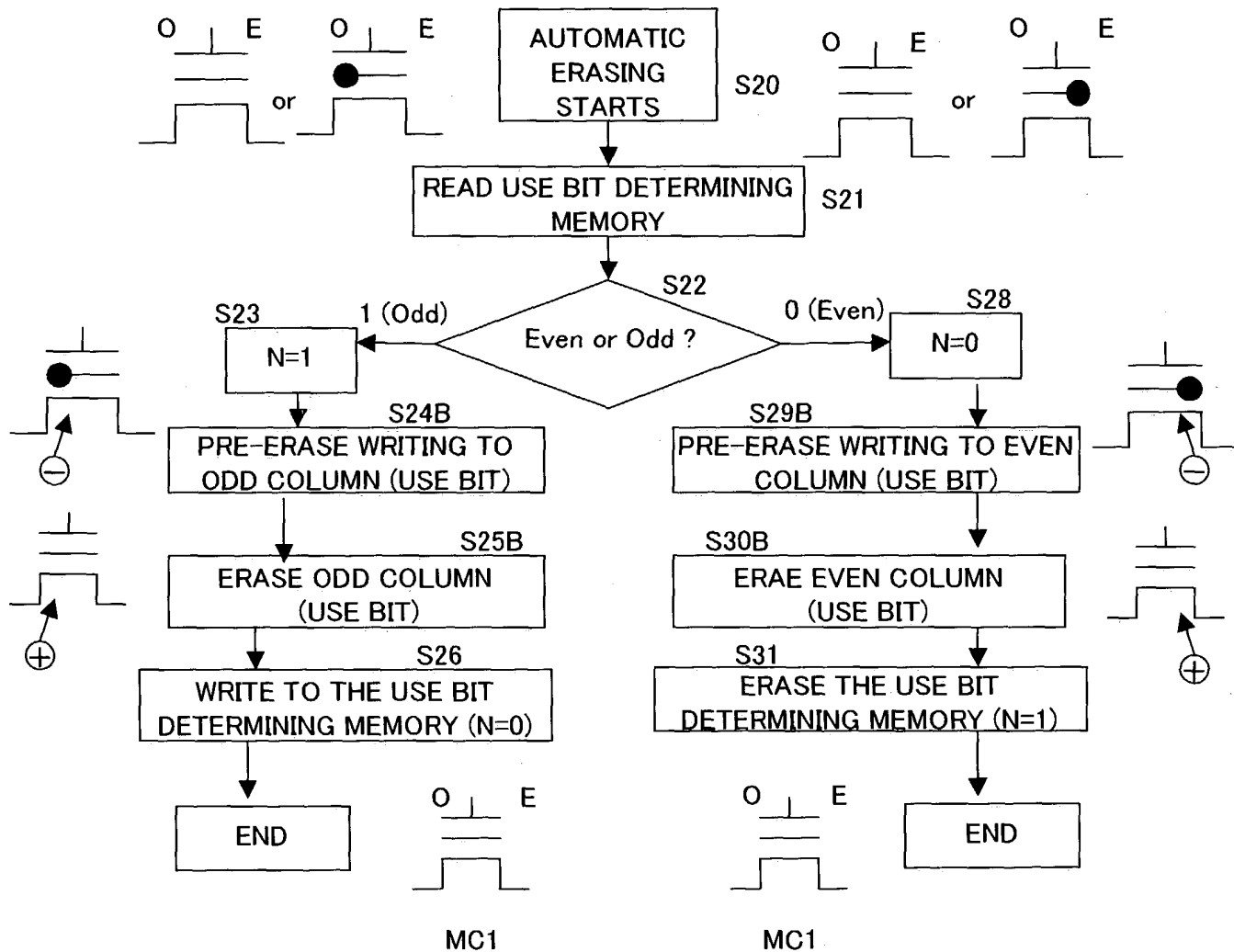


FIG. 22

AUTOMATIC ERASING OPERATION (2)  
WITH REPLACEMENT OF NON-USE BIT  
TO USE BIT, IN WHICH NON-USE BIT IS  
KEPT IN ERASED CONDITION

